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EXAMINER	
THANGAVELU, KANDASAMY	

ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,700	MOLSON ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to the Applicants' Amendment dated December 21, 2004. Claims 1, 2, 20, 21, 22, 23, 25, 27, 30 -32, 34 and 52-60 were amended. Claims 1-60 of the application are pending. This office action is made final.

Claim Objections

2. The following is a quotation of 37 C.F.R § 1.75 (d)(1):

> The claim or claims must conform to the invention as set forth in the remainder of the specification and terms and phrases in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

3. Claims 54-60 are objected to because of the following informalities:

Claim 54, Line 2, "the method comprising:" appears to be incorrect and it appears that it should be "the system comprising:"

Claim 56, Line 1, "(Original) The system of Claim 54" appears to be incorrect and it appears that it should be ""(Currently amended) The system of Claim 54".

Claim 57, Line 1, "(Original) The system of Claim 54" appears to be incorrect and it appears that it should be ""(Currently amended) The system of Claim 54".

Claim 58, Line 1, "(Original) The system of Claim 57" appears to be incorrect and it appears that it should be ""(Currently amended) The system of Claim 57".

Claim 59, Line 1, "(Original) The system of Claim 54" appears to be incorrect and it appears that it should be ""(Currently amended) The system of Claim 54".

Claim 60, Line 1, "(Original) The system of Claim 59" appears to be incorrect and it appears that it should be ""(Currently amended) The system of Claim 59".

Claims objected to but not specifically addressed are objected to based on their dependency to an objected claim.

Appropriate corrections are required.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 34-51 are rejected under 35 U.S.C. 101 because the claimed inventions are directed to non-statutory subject matter.

Independent claim 34 recites a computer program product associated with a computer readable medium including computer code for generating operationally limited hardware and software. The limitations recited in claim contain computer codes for executing various steps which are not statutory subject matter. To be statutory, the computer program product should include computer executable instructions which when executed in a computer performs a process comprising the steps included in the limitations.

Dependent claims 35-51 recite a computer program product. The limitations recited in

claim contain the features implemented in the computer program which are not statutory subject matter. To be statutory, the computer program product should include computer executable instructions which when executed in a computer performs a process comprising the steps included in the dependent claims.

6. Claims 34-51 would be allowable if claim 34 is rewritten as a computer program product associated with a computer readable medium including computer code **which when executed on a computer performs a process of** generating operationally limited hardware and software, ...

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Schneck et al.** (U.S. Patent Application 2001/0021926) in view of **Amano et al.** (U.S. Patent 6,557,020).

9.1 **Schneck et al.** teaches system for controlling access and distribution of digital property. Specifically, as per claim 1, **Schneck et al.** teaches a method for generating operationally limited software (Abstract, L7-17; Page 2, Para 0016; Page 4, Para 0044, Para 0045, and Para 0048; Page 10, Para 0154; Page 11, Para 0159); the method comprising:

identifying license information associated with a protected intellectual property block configured for implementation on a device (Abstract, L7-17; Page 2, Para 0016; Page 4, Para 0045, Para 0047 to Para 0050, Para 0052 to Para 0054; Fig. 3, Item 130; Page 6, Para 0097; Page 11, Para 0159);

generating operationally limited software, wherein the software is operationally limited using license information associated with the intellectual property block (Abstract, L7-17; Page 2, Para 0016; Page 4, Para 0045, Para 0048 to Para 0050, Para 0052, Para 0054; Fig. 3, Item 130; Page 6, Para 0097; Page 10, Para 0154; Page 11, Para 0159).

Schneck et al. does not expressly teach a method for generating operationally limited hardware, the method comprising: identifying license information associated with a protected intellectual property block configured for implementation on a device; generating operationally limited hardware, wherein the hardware is operationally limited using license information associated with the intellectual property block. **Amano et al.** teaches a method for generating

operationally limited hardware the method comprising: identifying license information associated with a protected intellectual property block configured for implementation on a device; generating operationally limited hardware, wherein the hardware is operationally limited using license information associated with the intellectual property block (CL7, L53-55; CL7, L65 to CL8, L8), because that allows hardware developers to incorporate various functional blocks developed by different manufacturers in the development of their ICs by obtaining license from the manufacturer of the functional block; the method simplifies the management of intellectual property rights (CL7, L53-55; CL7, L65 to CL8, L8). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Schneck et al.** with the method of **Amano et al.** that included a method for generating operationally limited hardware the method comprising: identifying license information associated with a protected intellectual property block configured for implementation on a device; generating operationally limited hardware, wherein the hardware is operationally limited using license information associated with the intellectual property block. The artisan would have been motivated because that would allow hardware developers to incorporate various functional blocks developed by different manufacturers in the development of their ICs by obtaining license from the manufacturer of the functional block; the method would simplify the management of intellectual property rights.

9.2 As per claim 54, **Schneck et al.** teaches a system for generating operationally limited software (Abstract, L7-17; Page 2, Para 0016; Page 4, Para 0044, Para 0045, and Para 0048; Page 10, Para 0154; Page 11, Para 0159); the method comprising:

means for identifying a protected intellectual property block associated with a design; means for identifying license information associated with the protected intellectual property block (Abstract, L7-17; Page 2, Para 0016; Page 4, Para 0045, Para 0047 to Para 0050, Para 0052 to Para 0054; Fig. 3, Item 130; Page 6, Para 0097; Page 11, Para 0159);

means for generating operationally limited software, wherein the software is operationally limited using license information (Abstract, L7-17; Page 2, Para 0016; Page 4, Para 0045, Para 0048 to Para 0050, Para 0052, Para 0054; Fig. 3, Item 130; Page 6, Para 0097; Page 10, Para 0154; Page 11, Para 0159).

Schneck et al. does not expressly teach a system for generating operationally limited hardware, the method comprising: means for identifying a protected intellectual property block associated with a design; means for identifying license information associated with the protected intellectual property block; means for generating operationally limited hardware, wherein the hardware is operationally limited using license information. **Amano et al.** teaches a system for generating operationally limited hardware, the method comprising: means for identifying a protected intellectual property block associated with a design; means for identifying license information associated with the protected intellectual property block; means for generating operationally limited hardware, wherein the hardware is operationally limited using license information (CL7, L53-55; CL7, L65 to CL8, L8), because that allows hardware developers to incorporate various functional blocks developed by different manufacturers in the development of their ICs by obtaining license from the manufacturer of the functional block; the method simplifies the management of intellectual property rights (CL7, L53-55; CL7, L65 to CL8, L8).

It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Schneck et al.** with the system of **Amano et al.** that included a system for generating operationally limited hardware, the method comprising: means for identifying a protected intellectual property block associated with a design; means for identifying license information associated with the protected intellectual property block; means for generating operationally limited hardware, wherein the hardware is operationally limited using license information. The artisan would have been motivated because that would allow hardware developers to incorporate various functional blocks developed by different manufacturers in the development of their ICs by obtaining license from the manufacturer of the functional block; the method would simplify the management of intellectual property rights.

10. Claims 2, 12, 13, 34, 44-45, 55 and 57-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Schneck et al.** (U.S. Patent Application 2001/0021926) in view of **Amano et al.** (U.S. Patent 6,557,020), and further in view of **Ginter et al.** (U.S. Patent 5,892,900).

10.1 As per claims 2, **Schneck et al.** and **Amano et al.** teach the method of claim 1. **Schneck et al.** does not expressly teach that the license information identifies a parameter associated with a prototype operation range and a production operation range. **Ginter et al.** teaches that the license information identifies a parameter associated with a prototype operation range and a production operation range (CL2, L66 to CL3, L3; CL3, L18-22; CL47, L66 to CL48, L31; CL56, L25-29; CL59, L42-52; CL59, L62 to CL 60, L3; CL140, L25-34; use for a limited time), because that would ensure the property providers proper compensation for the use of their

electronic information (CL2, L57-59); and allow the potential customers to use the software in a demonstration mode (prototype operation) and use the full program features (production operation) for a limited time without paying license fee; using a time based billing method, full use of the program for any period of time will be allowed (CL140,L25-38) . It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Schneck et al.** with the method of **Ginter et al.** that included the license information identifying a parameter associated with a prototype operation range and a production operation range. The artisan would have been motivated because that would ensure the property providers proper compensation for the use of their electronic information; allow the potential customers to use the software in a demonstration mode (prototype operation) and use the full program features (production operation) for a limited time without paying license fee; and using a time based billing method, full use of the program for any period of time would be allowed.

10.2 As per claims 12 and 13, **Schneck et al., Amano et al.** and **Ginter et al.** teach the method of claim 2. **Schneck et al.** does not expressly teach that the parameter is a software parameter; and the parameter is a time limit on run time during which the software will permit operation of the hardware. **Ginter et al.** teaches that the parameter is a software parameter; and the parameter is a time limit on run time during which the software will permit operation of the hardware (CL140, L25-34; use for a limited time), because that would ensure the property providers proper compensation for the use of their electronic information (CL2, L57-59); and allow the potential customers to use the software in a demonstration mode (prototype operation) and use the full program features (production operation) for a limited time without paying license

fee; using a time based billing method, full use of the program for any period of time will be allowed (CL140,L25-38). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Schneck et al.** with the method of **Ginter et al.** that included the parameter being a software parameter; and the parameter being a time limit on run time during which the software will permit operation of the hardware. The artisan would have been motivated because that would ensure the property providers proper compensation for the use of their electronic information; allow the potential customers to use the software in a demonstration mode (prototype operation) and use the full program features (production operation) for a limited time without paying license fee; and using a time based billing method, full use of the program for any period of time would be allowed.

10.3 As per claim 34, **Schneck et al.** teaches a computer program product associated with a computer readable medium including computer code for generating operationally limited software (Abstract, L7-17; Page 2, Para 0016; Page 4, Para 0044, Para 0045, and Para 0048; Page 10, Para 0154; Page 11, Para 0159); the computer program product comprising:

computer code for identifying a protected intellectual property block associated with a design (Abstract, L7-17; Page 2, Para 0016; Page 4, Para 0045, Para 0047 to Para 0050, Para 0052 to Para 0054; Fig. 3, Item 130; Page 6, Para 0097; Page 11, Para 0159);

computer code for generating operationally limited hardware and software (Abstract, L7-17; Page 2, Para 0016; Page 4, Para 0045, Para 0048 to Para 0050, Para 0052, Para 0054; Fig. 3, Item 130; Page 6, Para 0097; Page 10, Para 0154; Page 11, Para 0159).

Schneck et al. does not expressly teach a computer program product associated with a computer readable medium including computer code for generating operationally limited hardware; the computer program product comprising: computer code for identifying a protected intellectual property block associated with a design; and computer code for generating operationally limited hardware. **Amano et al.** teaches a computer program product associated with a computer readable medium including computer code for generating operationally limited hardware; the computer program product comprising: computer code for identifying a protected intellectual property block associated with a design; and computer code for generating operationally limited hardware (CL7, L53-55; CL7, L65 to CL8, L8), because that allows hardware developers to incorporate various functional blocks developed by different manufacturers in the development of their ICs by obtaining license from the manufacturer of the functional block; the method simplifies the management of intellectual property rights (CL7, L53-55; CL7, L65 to CL8, L8). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the computer program product of **Schneck et al.** with the computer program product of **Amano et al.** that included a computer program product associated with a computer readable medium including computer code for generating operationally limited hardware; the computer program product comprising: computer code for identifying a protected intellectual property block associated with a design; and computer code for generating operationally limited hardware. The artisan would have been motivated because that would allow hardware developers to incorporate various functional blocks developed by different manufacturers in the development of their ICs by obtaining license from the

manufacturer of the functional block; the method would simplify the management of intellectual property rights.

Schneck et al. does not expressly teach computer code for identifying a parameter using license information associated with the protected intellectual property block; and the hardware and software being operationally limited based on the parameter identified using license information. **Ginter et al.** teaches computer code for identifying a parameter using license information associated with the protected intellectual property block; and the hardware and software being operationally limited based on the parameter identified using license information (CL2, L66 to CL3, L3; CL3, L18-22; CL47, L66 to CL48, L31; CL56, L25-29; CL59, L42-52; CL59, L62 to CL 60, L3; CL140, L25-34; use for a limited time), because that would ensure the property providers proper compensation for the use of their electronic information (CL2, L57-59); and allow the potential customers to use the software and hardware in a demonstration mode (prototype operation) and use the full program features (production operation) for a limited time without paying license fee; using a time based billing method, full use of the program for any period of time will be allowed (CL140,L25-38) . It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the computer program product of **Schneck et al.** with the computer program product of **Ginter et al.** that included computer code for identifying a parameter using license information associated with the protected intellectual property block; and the hardware and software being operationally limited based on the parameter identified using license information. The artisan would have been motivated because that would ensure the property providers proper compensation for the use of their electronic information; allow the potential customers to use the software in a demonstration mode

(prototype operation) and use the full program features (production operation) for a limited time without paying license fee; and using a time based billing method, full use of the program for any period of time would be allowed.

10.4 As per Claims 44 and 45, these are rejected based on the same reasoning as Claims 12 and 13, supra. Claims 44 and 45 are computer program product claims reciting the same limitations as Claims 12 and 13, as taught throughout by **Schneck et al., Amano et al., Ginter et al.**

10.5 As per claim 55, **Schneck et al., Amano et al.** and **Ginter et al.** teach the system of claim 54. **Schneck et al.** does not expressly teach that the license information comprises a first operation range and a second operation range. **Ginter et al.** teaches that the license information comprises a first operation range and a second operation range (CL2, L66 to CL3, L3; CL3, L18-22; CL47, L66 to CL48, L31; CL56, L25-29; CL59, L42-52; CL59, L62 to CL 60, L3; CL140, L25-34; use for a limited time), because that would ensure the property providers proper compensation for the use of their electronic information (CL2, L57-59); and allow the potential customers to use the software in a demonstration mode (prototype operation) and use the full program features (production operation) for a limited time without paying license fee; using a time based billing method, full use of the program for any period of time will be allowed (CL140,L25-38) . It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Schneck et al.** with the system of **Ginter et al.** that included the license information comprising a first operation range and a second operation

range. The artisan would have been motivated because that would ensure the property providers proper compensation for the use of their electronic information; allow the potential customers to use the software in a demonstration mode (prototype operation) and use the full program features (production operation) for a limited time without paying license fee; and using a time based billing method, full use of the program for any period of time would be allowed.

10.6 As per claim 57, **Schneck et al., Amano et al.** and **Ginter et al.** teach the system of claim 54. **Schneck et al.** does not expressly teach that the operational parameter is time and further wherein the first operation range is a prototype testing time range and the second operation range is a production time range. **Ginter et al.** teaches that the operational parameter is time and further wherein the first operation range is a prototype testing time range and the second operation range is a production time range (CL2, L66 to CL3, L3; CL3, L18-22; CL47, L66 to CL48, L31; CL56, L25-29; CL59, L42-52; CL59, L62 to CL 60, L3; CL140, L25-34; use for a limited time), because that would ensure the property providers proper compensation for the use of their electronic information (CL2, L57-59); and allow the potential customers to use the software in a demonstration mode (prototype operation) and use the full program features (production operation) for a limited time without paying license fee; using a time based billing method, full use of the program for any period of time will be allowed (CL140,L25-38) . It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Schneck et al.** with the system of **Ginter et al.** that included the operational parameter is time and further wherein the first operation range is a prototype testing time range and the second operation range is a production time range. The artisan would have

been motivated because that would ensure the property providers proper compensation for the use of their electronic information; allow the potential customers to use the software in a demonstration mode (prototype operation) and use the full program features (production operation) for a limited time without paying license fee; and using a time based billing method, full use of the program for any period of time would be allowed.

10.7 As per claims 58-60, **Schneck et al., Amano et al.** and **Ginter et al.** teach the system of claim 57. **Schneck et al.** does not expressly teach that the prototype testing time range has a maximum and further wherein the production time range has no maximum; the first operation range is a range of timed operation having a maximum time limit and wherein the second operation range is a range of timed operation extending beyond the maximum time limit; and the second operation range has no maximum time limit. **Ginter et al.** teaches that that the prototype testing time range has a maximum and further wherein the production time range has no maximum; the first operation range is a range of timed operation having a maximum time limit and wherein the second operation range is a range of timed operation extending beyond the maximum time limit; and the second operation range has no maximum time limit (CL3, L13-29; CL7, L42-45), because that would ensure the property providers proper compensation for the use of their electronic information (CL2, L57-59); and allow the potential customers to use the software in a demonstration mode (prototype operation) and use the full program features (production operation) for a limited time without paying license fee; using a time based billing method, full use of the program for any period of time will be allowed (CL140,L25-38) . It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to

modify the system of **Schneck et al.** with the system of **Ginter et al.** that included the prototype testing time range having a maximum and further wherein the production time range had no maximum; the first operation range was a range of timed operation having a maximum time limit and wherein the second operation range was a range of timed operation extending beyond the maximum time limit; and the second operation range had no maximum time limit. The artisan would have been motivated because that would ensure the property providers proper compensation for the use of their electronic information; allow the potential customers to use the software in a demonstration mode (prototype operation) and use the full program features (production operation) for a limited time without paying license fee; and using a time based billing method, full use of the program for any period of time would be allowed.

11. Claims 3, 19, 35, 51 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Schneck et al.** (U.S. Patent Application 2001/0021926) in view of **Amano et al.** (U.S. Patent 6,557,020), and further in view of **Ginter et al.** (U.S. Patent 5,892,900) and **Gardner et al.** (U.S. Patent 6,346,427).

11.1 As per claim 3, **Schneck et al., Amano et al.** and **Ginter et al.** teach the method of claim 2. **Schneck et al.** does not expressly teach that the parameter is a hardware parameter. **Gardner et al.** teaches that the parameter is a hardware parameter (Abstract, L1-4; CL4, L36-40), because that would allow tuning the parameters of the product after the prototype verification, thus decreasing the cost of the fabrication process (CL4, L36-39). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Schneck**

et al. with the method of **Gardner et al.** that included the parameter being a hardware parameter. The artisan would have been motivated because that would allow tuning the parameters of the product after the prototype verification, thus decreasing the cost of the fabrication process.

11.2 As per claim 19, **Schneck et al., Amano et al., Ginter et al.** and **Gardner et al.** teach the method of claim 2. **Schneck et al.** does not expressly teach that the step of identifying a parameter comprises the step of identifying multiple parameters in accordance with the identification step and further wherein the step of limiting operation of the hardware and software comprises the step of limiting operation of the hardware and software with regard to each identified parameter in accordance with the limitation step. **Gardner et al.** teaches that the step of identifying a parameter comprises the step of identifying multiple parameters in accordance with the identification step and further wherein the step of limiting operation of the hardware and software comprises the step of limiting operation of the hardware and software with regard to each identified parameter in accordance with the limitation step (Abstract, L1-4; CL4, L36-40), because that would allow tuning the parameters of the product after the prototype verification of the gate arrays (CL4, L36-39). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Schneck et al.** with the method of **Gardner et al.** that included the step of identifying a parameter comprising the step of identifying multiple parameters in accordance with the identification step and further wherein the step of limiting operation of the hardware and software comprising the step of limiting operation of the hardware and software with regard to each identified parameter in

accordance with the limitation step. The artisan would have been motivated because that would allow tuning the parameters of the product after the prototype verification of the gate arrays.

11.3 As per Claim 35, it is rejected based on the same reasoning as Claim 3, supra. Claim 35 is a computer program product claim reciting the same limitations as Claim 3, as taught throughout by **Schneck et al., Amano et al., Ginter et al.** and **Gardner et al.**

11.4 As per Claim 51, it is rejected based on the same reasoning as Claim 19, supra. Claim 51 is a computer program product claim reciting the same limitations as Claim 19, as taught throughout by **Schneck et al., Amano et al., Ginter et al.** and **Gardner et al**

11.5 As per claim 56, **Schneck et al., Amano et al.** and **Ginter et al.** teach the system of claim 54. **Schneck et al.** does not expressly teach that the first operation range and the second operation range are mutually exclusive. **Gardner et al.** teaches that the first operation range and the second operation range are mutually exclusive (Abstract, L1-4; CL4, L36-40), because that would allow tuning the parameters of the product after the prototype verification of the gate arrays, thus decreasing the cost of the fabrication process (CL4, L36-39). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the system of **Schneck et al.** with the system of **Gardner et al.** that included the first operation range and the second operation range being mutually exclusive. The artisan would have been motivated because that would allow tuning the parameters of the product after the prototype verification of the gate arrays, thus decreasing the cost of the fabrication process.

12. Claims 4 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Schneck et al.** (U.S. Patent Application 2001/0021926) in view of **Amano et al.** (U.S. Patent 6,557,020), and further in view of **Ginter et al.** (U.S. Patent 5,892,900), **Gardner et al.** (U.S. Patent 6,346,427) and **Hurvig et al.** (U.S. Patent 6,507,592).

12.1 As per claim 4, **Schneck et al., Amano et al., Ginter et al.** and **Gardner et al.** teach the method of claim 3. **Schneck et al.** does not expressly teach that the hardware parameter is a data format. **Hurvig et al.** teaches that the hardware parameter is a data format (CL14, L3-5), because the circuitry may be specific to the data format (CL14, L3-5). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Schneck et al.** with the method of **Hurvig et al.** that included the hardware parameter being a data format. The artisan would have been motivated because the circuitry might be specific to the data format.

12.2 As per Claim 36, it is rejected based on the same reasoning as Claim 4, supra. Claim 36 is a computer program product claim reciting the same limitations as Claim 4, as taught throughout by **Schneck et al., Amano et al., Ginter et al., Gardner et al.** and **Hurvig et al.**

13. Claims 5-8, 20, 21, 37-40 and 52-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Schneck et al.** (U.S. Patent Application 2001/0021926) in view of **Amano et**

al. (U.S. Patent 6,557,020), and further in view of **Ginter et al.** (U.S. Patent 5,892,900), **Gardner et al.** (U.S. Patent 6,346,427) and **Lin** (U.S. Patent 6,421,251).

13.1 As per claim 5, **Schneck et al., Amano et al., Ginter et al.** and **Gardner et al.** teach the method of claim 3. **Schneck et al.** does not expressly teach that the hardware parameter is the number of pin contacts between the hardware and an external device. **Lin** teaches that the hardware parameter is the number of pin contacts between the hardware and an external device (CL6, L63-64; CL29, L31-32; CL30, L7-9), because the number of pins used vary from chip to chip based on the location of the interconnections on the board (CL6, L67 to CL7, L1); and the number of pin usage is minimized (CL29, L13). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Schneck et al.** with the method of **Lin** that included the hardware parameter being the number of pin contacts between the hardware and an external device. The artisan would have been motivated because the number of pins used would vary from chip to chip based on the location of the interconnections on the board; and the number of pin usage would be minimized.

13.2 As per claims 6-8, **Schneck et al., Amano et al., Ginter et al.** and **Gardner et al.** teach the method of claim 3. **Schneck et al.** does not expressly teach that the hardware parameter is a signal limit; the signal limit is a limit on the number of input signals allowed into the hardware by the software; and the signal limit is a limit on the number of output signals allowed out of the hardware by the software. **Lin** teaches that the hardware parameter is a signal limit; the signal limit is a limit on the number of input signals allowed into the hardware by the software; and the

signal limit is a limit on the number of output signals allowed out of the hardware by the software (CL32, L1-5), because the number of signals determine the I/O capacity required and the number of signals that should be routed through longer paths than shortest paths (CL32, L1-5). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Schneck et al.** with the method of **Lin** that included the hardware parameter being a signal limit; the signal limit being a limit on the number of input signals allowed into the hardware by the software; and the signal limit being a limit on the number of output signals allowed out of the hardware by the software. The artisan would have been motivated because the number of signals would determine the I/O capacity required and the number of signals that should be routed through longer paths than shortest paths.

13.3 As per claims 20 and 21, **Schneck et al., Amano et al.** and **Ginter et al.** teach the method of claim 2. **Schneck et al.** does not expressly teach that the intellectual property block is implemented on a programmable chip; and the programmable chip is a programmable logic device. **Lin** teaches that the intellectual property block is implemented on a programmable chip; and the programmable chip is a programmable logic device (CL57, L28-35), because the programmable logic devices contain embedded array blocks and logic array blocks which can be used to implement various memory and complex logic functions (CL57, L36-40). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Schneck et al.** with the method of **Lin** that included the intellectual property block being implemented on a programmable chip; and the programmable chip being a programmable logic device. The artisan would have been motivated because the programmable logic devices

would contain embedded array blocks and logic array blocks which could be used to implement various memory and complex logic functions.

13.4 As per Claims 37-40, these are rejected based on the same reasoning as Claim 5-8, supra. Claims 37-40 are computer program product claims reciting the same limitations as Claim 4, as taught throughout by **Schneck et al., Amano et al., Ginter et al., Gardner et al.** and **Lin.**

13.5 As per Claims 52 and 53, these are rejected based on the same reasoning as Claims 20 and 21, supra. Claims 52 and 53 are computer program product claims reciting the same limitations as Claims 20 and 21, as taught throughout by **Schneck et al., Amano et al., Ginter et al. Gardner et al.** and **Lin.**

14. Claims 9 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Schneck et al.** (U.S. Patent Application 2001/0021926) in view of **Amano et al.** (U.S. Patent 6,557,020), and further in view of **Ginter et al.** (U.S. Patent 5,892,900), **Gardner et al.** (U.S. Patent 6,346,427), **Hurvig et al.** (U.S. Patent 6,507,592) and **Lin** (U.S. Patent 6,421,251).

14.1 As per claim 9, **Schneck et al., Amano et al., Ginter et al., Gardner et al.** and **Lin** teach the method of claim 8. **Schneck et al.** does not expressly teach that the output signals are signals used to provide the status of either the hardware or the software. **Hurvig et al.** teaches that the output signals are signals used to provide the status of either the hardware or the software (CL14, L37-40; CL17, L48-52), because the hardware or software status signals are

used to generate interrupt to the CPU (CL14, L37-40). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Schneck et al.** with the method of **Hurvig et al.** that included the output signals being signals used to provide the status of either the hardware or the software. The artisan would have been motivated because the hardware or software status signals would be used to generate interrupt to the CPU.

14.2 As per Claim 41, it is rejected based on the same reasoning as Claim 9, supra. Claim 41 is a computer program product claim reciting the same limitations as Claim 9, as taught throughout by **Schneck et al., Amano et al., Ginter et al., Gardner et al., Hurvig et al.** and **Lin.**

15. Claims 10 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Schneck et al.** (U.S. Patent Application 2001/0021926) in view of **Amano et al.** (U.S. Patent 6,557,020), and further in view of **Ginter et al.** (U.S. Patent 5,892,900), **Gardner et al.** (U.S. Patent 6,346,427) and **Gee et al.** (U.S. Patent 6,317,872).

15.1 As per claim 10, **Schneck et al., Amano et al., Ginter et al.** and **Gardner et al.** teach the method of claim 3. **Schneck et al.** does not expressly teach that the parameter is limited by preselected fabrication of the hardware. **Gee et al.** teaches that the parameter is limited by preselected fabrication of the hardware (CL20, L25-28), because the hardware characteristics of the system are dictated by physical fabrication parameters (CL20, L25-28). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the

method of **Schneck et al.** with the method of **Gee et al.** that included the parameter being limited by preselected fabrication of the hardware. The artisan would have been motivated because the hardware characteristics of the system would be dictated by physical fabrication parameters.

15.2 As per Claim 42, it is rejected based on the same reasoning as Claim 10, supra. Claim 42 is a computer program product claim reciting the same limitations as Claim 10, as taught throughout by **Schneck et al., Amano et al., Ginter et al., Gardner et al.** and **Gee et al.**

16. Claims 11 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Schneck et al.** (U.S. Patent Application 2001/0021926) in view of **Amano et al.** (U.S. Patent 6,557,020), and further in view of **Ginter et al.** (U.S. Patent 5,892,900), **Gardner et al.** (U.S. Patent 6,346,427) and **Walker** (U.S. Patent 6,157,317).

16.1 As per claim 11, **Schneck et al., Amano et al., Ginter et al.** and **Gardner et al.** teach the method of claim 3. **Schneck et al.** does not expressly teach that the parameter is limited by preselected augmentation of the hardware. **Walker** teaches that the parameter is limited by preselected augmentation of the hardware (CL21, L4-6), because the hardware augmentation can be performed through future modular hardware changes to affect performance (CL21, L4-6). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Schneck et al.** with the method of **Walker** that included the parameter being limited by preselected augmentation of the hardware. The artisan would have been

motivated because the hardware augmentation could be performed through future modular hardware changes to affect performance.

16.2 As per Claim 43, it is rejected based on the same reasoning as Claim 11, supra. Claim 43 is a computer program product claim reciting the same limitations as Claim 11, as taught throughout by **Schneck et al., Amano et al., Ginter et al., Gardner et al.** and **Walker.**

17. Claims 14 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Schneck et al.** (U.S. Patent Application 2001/0021926) in view of **Amano et al.** (U.S. Patent 6,557,020), and further in view of **Ginter et al.** (U.S. Patent 5,892,900) and **Mueller et al.** (U.S. Patent Re. 31,736).

17.1 As per claim 14, **Schneck et al., Amano et al.** and **Ginter et al.** teach the method of claim 13. **Schneck et al.** does not expressly teach the step of disabling the hardware after the time limit has been attained. **Mueller et al.** teaches the step of disabling the hardware after the time limit has been attained (CL1, L50-52), because that allows a timer or score counting circuit to disable the hardware operation after a preset time limit or number of points scored (CL1, L50-52). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Schneck et al.** with the method of **Mueller et al.** that included the step of disabling the hardware after the time limit has been attained. The artisan would have been motivated because that would allow a timer or score counting circuit to disable the hardware operation after a preset time limit or number of points scored.

17.2 As per Claim 46, it is rejected based on the same reasoning as Claim 14, supra. Claim 46 is a computer program product claim reciting the same limitations as Claim 14, as taught throughout by **Schneck et al., Amano et al., Ginter et al.** and **Mueller et al.**

18. Claims 15 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Schneck et al.** (U.S. Patent Application 2001/0021926) in view of **Amano et al.** (U.S. Patent 6,557,020), and further in view of **Ginter et al.** (U.S. Patent 5,892,900), **Mueller et al.** (U.S. Patent Re. 31,736) and **Lin** (U.S. Patent 6,421,251).

18.1 As per claim 15, **Schneck et al., Amano et al., Ginter et al.** and **Mueller et al.** teach the method of claim 14. **Schneck et al.** does not expressly teach that the step of disabling the hardware comprises a reset of a register in the hardware. **Lin** teaches that the step of disabling the hardware comprises a reset of a register in the hardware (CL55, L11-14; CL55, L55-57), because that ensures that the output signals are logic "0" thus removing the enable signal from the hardware register model (CL55, L11-14; CL55, L55-57). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Schneck et al.** with the method of **Lin** that included the step of disabling the hardware comprising a reset of a register in the hardware. The artisan would have been motivated because that would ensure that the output signals were logic "0" thus removing the enable signal from the hardware register model.

18.2 As per Claim 47, it is rejected based on the same reasoning as Claim 15, supra. Claim 47 is a computer program product claim reciting the same limitations as Claim 15, as taught throughout by **Schneck et al., Amano et al., Ginter et al., Mueller et al.** and **Lin.**

19. Claims 16 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Schneck et al.** (U.S. Patent Application 2001/0021926) in view of **Amano et al.** (U.S. Patent 6,557,020), and further in view of **Ginter et al.** (U.S. Patent 5,892,900), **Mueller et al.** (U.S. Patent Re. 31,736) and **Ngai et al.** (U.S. Patent 6,480,027).

19.1 As per claim 16, **Schneck et al., Amano et al., Ginter et al.** and **Mueller et al.** teach the method of claim 14. **Schneck et al.** does not expressly teach that disabling the hardware comprises a global tri-state of the hardware I/O. **Ngai et al.** teaches that disabling the hardware comprises a global tri-state of the hardware I/O (CL7, L26-35), because that allows selectively driving signals from input pins or input/output pins or adjacent logic regions onto conductor segments or vice versa (CL7, L28-32). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Schneck et al.** with the method of **Ngai et al.** that included disabling the hardware comprising a global tri-state of the hardware I/O. The artisan would have been motivated because that would allow selectively driving signals from input pins or input/output pins or adjacent logic regions onto conductor segments or vice versa.

19.2 As per Claim 48, it is rejected based on the same reasoning as Claim 16, supra. Claim 48 is a computer program product claim reciting the same limitations as Claim 16, as taught throughout by **Schneck et al., Amano et al., Ginter et al., Mueller et al.** and **Ngai et al.**

20. Claims 17 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Schneck et al.** (U.S. Patent Application 2001/0021926) in view of **Amano et al.** (U.S. Patent 6,557,020), and further in view of **Ginter et al.** (U.S. Patent 5,892,900), **Mueller et al.** (U.S. Patent Re. 31,736) and **Watson et al.** (U.S. Patent 5,982,683).

20.1 As per claim 17, **Schneck et al., Amano et al., Ginter et al.** and **Mueller et al.** teach the method of claim 14. **Schneck et al.** does not expressly teach that disabling the hardware comprises a random failure of the hardware. **Watson et al.** teaches that disabling the hardware comprises a random failure of the hardware (CL6, L20-24), because the likely occurrence of a failure in random chance would be in the interconnect harness, the macrocells, the programmable logic and in the related products (CL6, L20-24). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Schneck et al.** with the method of **Watson et al.** that included disabling the hardware comprising a random failure of the hardware. The artisan would have been motivated because the likely occurrence of a failure in random chance would be in the interconnect harness, the macrocells, the programmable logic and in the related products.

20.2 As per Claim 49, it is rejected based on the same reasoning as Claim 17, supra. Claim 49 is a computer program product claim reciting the same limitations as Claim 17, as taught throughout by **Schneck et al., Amano et al., Ginter et al., Mueller et al.** and **Watson et al.**

21. Claims 18 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Schneck et al.** (U.S. Patent Application 2001/0021926) in view of **Amano et al.** (U.S. Patent 6,557,020), and further in view of **Ginter et al.** (U.S. Patent 5,892,900), **Mueller et al.** (U.S. Patent Re. 31,736), **Lin** (U.S. Patent 6,421,251) and **DeRoo et al.** (U.S. Patent 5,802,376).

21.1 As per claim 18, **Schneck et al., Amano et al., Ginter et al.** and **Mueller et al.** teach the method of claim 14. **Schneck et al.** does not expressly teach that an internal clock of the hardware is used to measure the run time of the hardware. **Lin** teaches that an internal clock of the hardware is used (CL48, L3-4; CL49, L7-9), because that reduces the number of software clocks required in the system (CL49, L7-9). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Schneck et al.** with the method of **Lin** that included an internal clock of the hardware being used. The artisan would have been motivated because that would reduce the number of software clocks required in the system.

Schneck et al. does not expressly teach that an internal clock of the hardware is used to measure the run time of the hardware. **DeRoo et al.** teaches that an internal clock of the hardware is used to measure the run time of the hardware (CL73, L65 to CL74, L6), because the programmable hardware timers allow predetermined time intervals to be programmed for a wide

range of performance levels (CL73, L65 to CL74, L2). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Schneck et al.** with the method of **DeRoo et al.** that included an internal clock of the hardware being used to measure the run time of the hardware. The artisan would have been motivated because the programmable hardware timers would allow predetermined time intervals to be programmed for a wide range of performance levels.

21.2 As per Claim 50, it is rejected based on the same reasoning as Claim 18, supra. Claim 50 is a computer program product claim reciting the same limitations as Claim 18, as taught throughout by **Schneck et al., Amano et al., Ginter et al., Mueller et al., Lin** and **DeRoo et al.**

22. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Mueller et al.** (U.S. Patent Re. 31,736) in view of **Winkelman** (U.S. Patent 4,435,752), and further in view of **DeRoo et al.** (U.S. Patent 5,802,376) and **Ginter et al.** (U.S. Patent 5,892,900).

22.1 As per claim 22, **Mueller et al.** teaches a method for disabling a hardware device (CL1, L50-52); the method comprising:

disabling the hardware after the time elapsed reaches the run time limit (CL1, L50-52).

Mueller et al. does not expressly teach identifying a run time limit that is (i) long enough to permit testing of the hardware in a prototype manner and (ii) too short for use of the hardware in a production manner. **Winkelman** teaches identifying a run time limit that is (i) long enough

to permit testing of the hardware in a prototype manner and (ii) too short for use of the hardware in a production manner (CL21, L58-65), because that would allow using steps to force from execution certain functions when they have exceeded a given time limit (CL21, L61-63). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Mueller et al.** with the method of **Winkelman** that included identifying a run time limit that was (i) long enough to permit testing of the hardware in a prototype manner and (ii) too short for use of the hardware in a production manner. The artisan would have been motivated because that would allow using steps to force from execution certain functions when they have exceeded a given time limit.

Mueller et al. does not expressly teach that the run time limit is configured at least in part using license information associated with a protected intellectual property block implemented on a hardware device. **Ginter et al.** teaches that the run time limit is configured at least in part using license information associated with a protected intellectual property block implemented on a hardware device (CL2, L66 to CL3, L3; CL3, L18-22; CL47, L66 to CL48, L31; CL56, L25-29; CL59, L42-52; CL59, L62 to CL 60, L3; CL140, L25-34; use for a limited time), because that would ensure the property providers proper compensation for the use of their electronic information (CL2, L57-59); and allow the potential customers to use the software in a demonstration mode (prototype operation) and use the full program features (production operation) for a limited time without paying license fee; using a time based billing method, full use of the program for any period of time will be allowed (CL140,L25-38) . It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Mueller et al.** with the method of **Ginter et al.** that included the run time limit being

configured at least in part using license information associated with a protected intellectual property block implemented on a hardware device. The artisan would have been motivated because that would ensure the property providers proper compensation for the use of their electronic information; allow the potential customers to use the software in a demonstration mode (prototype operation) and use the full program features (production operation) for a limited time without paying license fee; and using a time based billing method, full use of the program for any period of time would be allowed.

Mueller et al. does not expressly teach measuring the time elapsed during operation of the hardware. **DeRoo et al.** teaches measuring the time elapsed during operation of the hardware (CL73, L65 to CL74, L6), because the programmable hardware timers allow counting the time elapsed using predetermined time intervals programmed for a wide range of performance levels (CL73, L65 to CL74, L2). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Mueller et al.** with the method of **DeRoo et al.** that included measuring the time elapsed during operation of the hardware. The artisan would have been motivated because the programmable hardware timers would allow counting the time elapsed using predetermined time intervals programmed for a wide range of performance levels.

23. Claims 23, 24, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Mueller et al.** (U.S. Patent Re. 31,736) in view of **Winkelman** (U.S. Patent 4,435,752), and further in view of **DeRoo et al.** (U.S. Patent 5,802,376), **Ginter et al.** (U.S. Patent 5,892,900)) and **Lin** (U.S. Patent 6,421,251).

23.1 As per claim 23, **Mueller et al., Winkelman, DeRoo et al.** and **Ginter et al.** teach the method of claim 22. **Mueller et al.** does not expressly teach that measuring the time elapsed is performed by an internal clock within the hardware. **Lin** teaches that measuring the time elapsed is performed by an internal clock within the hardware (CL48, L3-4; CL49, L7-9), because that reduces the number of software clocks required in the system (CL49, L7-9). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Mueller et al.** with the method of **Lin** that included measuring the time elapsed being performed by an internal clock within the hardware. The artisan would have been motivated because that would reduce the number of software clocks required in the system.

23.2 As per claim 24, **Mueller et al., Winkelman, DeRoo et al.** and **Ginter et al.** teach the method of claim 22. **Mueller et al.** does not expressly teach that disabling the hardware comprises a reset of a register in the hardware. **Lin** teaches that disabling the hardware comprises a reset of a register in the hardware (CL55, L11-14; CL55, L55-57), because that ensures that the output signals are logic "0" thus removing the enable signal from the hardware register model (CL55, L11-14; CL55, L55-57). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Mueller et al.** with the method of **Lin** that included disabling the hardware comprising a reset of a register in the hardware. The artisan would have been motivated because that would ensure that the output signals were logic "0" thus removing the enable signal from the hardware register model.

23.3 As per claim 28, **Mueller et al., Winkelman, DeRoo et al.** and **Ginter et al.** teach the method of claim 22. **Schneck et al.** does not expressly teach a hardware device implementing the method of claim 22; and the device is a programmable logic device. **Lin** teaches a hardware device implementing the method of claim 22; and the device is a programmable logic device (CL57, L28-35), because the programmable logic devices contain embedded array blocks and logic array blocks which can be used to implement various memory and complex logic functions (CL57, L36-40). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the hardware device of **Schneck et al.** with the hardware device of **Lin** that included a hardware device implementing the method of claim 22; and the device being a programmable logic device. The artisan would have been motivated because the programmable logic devices would contain embedded array blocks and logic array blocks which could be used to implement various memory and complex logic functions.

24. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Mueller et al.** (U.S. Patent Re. 31,736) in view of **Winkelman** (U.S. Patent 4,435,752), and further in view of **DeRoo et al.** (U.S. Patent 5,802,376), **Ginter et al.** (U.S. Patent 5,892,900) and **Ngai et al.** (U.S. Patent 6,480,027).

24.1 As per claim 25, **Mueller et al., Winkelman, DeRoo et al.** and **Ginter et al.** teach the method of claim 22. **Mueller et al.** does not expressly teach that disabling the hardware comprises a global tri-state of the hardware I/O. **Ngai et al.** teaches that disabling the hardware comprises a global tri-state of the hardware I/O (CL7, L26-35), because that allows selectively

driving signals from input pins or input/output pins or adjacent logic regions onto conductor segments or vice versa (CL7, L28-32). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Mueller et al.** with the method of **Ngai et al.** that included disabling the hardware comprising a global tri-state of the hardware I/O. The artisan would have been motivated because that would allow selectively driving signals from input pins or input/output pins or adjacent logic regions onto conductor segments or vice versa.

25. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Mueller et al.** (U.S. Patent Re. 31,736) in view of **Winkelman** (U.S. Patent 4,435,752), and further in view of **DeRoo et al.** (U.S. Patent 5,802,376), **Ginter et al.** (U.S. Patent 5,892,900) and **Watson et al.** (U.S. Patent 5,982,683).

25.1 As per claim 26, **Mueller et al., Winkelman, DeRoo et al.** and **Ginter et al.** teach the method of claim 22. **Mueller et al.** does not expressly teach that disabling the hardware comprises a random failure of the hardware. **Watson et al.** teaches that disabling the hardware comprises a random failure of the hardware (CL6, L20-24), because the likely occurrence of a failure in random chance would be in the interconnect harness, the macrocells, the programmable logic and in the related products (CL6, L20-24). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Mueller et al.** with the method of **Watson et al.** that included disabling the hardware comprising a random failure of the hardware. The artisan would have been motivated because the likely occurrence of a failure

in random chance would be in the interconnect harness, the macrocells, the programmable logic and in the related products.

26. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Mueller et al.** (U.S. Patent Re. 31,736) in view of **Winkelman** (U.S. Patent 4,435,752), and further in view of **DeRoo et al.** (U.S. Patent 5,802,376), **Ginter et al.** (U.S. Patent 5,892,900), **Lin** (U.S. Patent 6,421,251), **Ngai et al.** (U.S. Patent 6,480,027) and **Watson et al.** (U.S. Patent 5,982,683).

26.1 As per claim 27, **Mueller et al., Winkelman, DeRoo et al.** and **Ginter et al.** teach the method of claim 22. **Mueller et al.** does not expressly teach that disabling is selected from a reset of a register in the hardware. **Lin** teaches that disabling is selected from a reset of a register in the hardware (CL55, L11-14; CL55, L55-57), because that ensures that the output signals are logic "0" thus removing the enable signal from the hardware register model (CL55, L11-14; CL55, L55-57). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Mueller et al.** with the method of **Lin** that included disabling being selected from a reset of a register in the hardware. The artisan would have been motivated because that would ensure that the output signals were logic "0" thus removing the enable signal from the hardware register model.

Mueller et al. does not expressly teach that disabling is selected from a global tri-state of the I/O of the hardware. **Ngai et al.** teaches that disabling is selected from a global tri-state of the I/O of the hardware (CL7, L26-35), because that allows selectively driving signals from input pins or input/output pins or adjacent logic regions onto conductor segments or vice versa (CL7,

L28-32). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Mueller et al.** with the method of **Ngai et al.** that included disabling being selected from a global tri-state of the I/O of the hardware. The artisan would have been motivated because that would allow selectively driving signals from input pins or input/output pins or adjacent logic regions onto conductor segments or vice versa.

Mueller et al. does not expressly teach that disabling is selected from a random failure within the hardware. **Watson et al.** teaches that disabling is selected from a random failure within the hardware (CL6, L20-24), because the likely occurrence of a failure in random chance would be in the interconnect harness, the macrocells, the programmable logic and in the related products (CL6, L20-24). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Mueller et al.** with the method of **Watson et al.** that included disabling being selected from a random failure within the hardware. The artisan would have been motivated because the likely occurrence of a failure in random chance would be in the interconnect harness, the macrocells, the programmable logic and in the related products.

27. Claims 30, 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over **DeRoo et al.** (U.S. Patent 5,802,376), in view of **Winkelman** (U.S. Patent 4,435,752), and further in view of **Ginter et al.** (U.S. Patent 5,892,900) and **Mueller et al.** (U.S. Patent Re. 31,736).

27.1 As per claim 30, **DeRoo et al.** teaches counter in a hardware device, comprising a clock and a memory containing a run time limit measured by the clock (CL73, L65 to CL74, L6).

DeRoo et al. does not expressly teach the run time limit being (i) long enough to permit testing of the hardware in a prototype manner and (ii) too short for use of the hardware in a production manner. **Winkelman** teaches the run time limit being (i) long enough to permit testing of the hardware in a prototype manner and (ii) too short for use of the hardware in a production manner (CL21, L58-65), because that would allow using steps to force from execution certain functions when they have exceeded a given time limit (CL21, L61-63). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the hardware device of **DeRoo et al.** with the hardware device of **Winkelman** that included the run time limit being (i) long enough to permit testing of the hardware in a prototype manner and (ii) too short for use of the hardware in a production manner. The artisan would have been motivated because that would allow using steps to force from execution certain functions when they have exceeded a given time limit.

DeRoo et al. does not expressly teach that the run time limit is configured at least in part using license information associated with a protected intellectual property block implemented on a hardware device. **Ginter et al.** teaches that the run time limit is configured at least in part using license information associated with a protected intellectual property block implemented on a hardware device (CL2, L66 to CL3, L3; CL3, L18-22; CL47, L66 to CL48, L31; CL56, L25-29; CL59, L42-52; CL59, L62 to CL 60, L3; CL140, L25-34; use for a limited time), because that would ensure the property providers proper compensation for the use of their electronic information (CL2, L57-59); and allow the potential customers to use the software in a

demonstration mode (prototype operation) and use the full program features (production operation) for a limited time without paying license fee; using a time based billing method, full use of the program for any period of time will be allowed (CL140,L25-38) . It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the hardware device of **DeRoo et al.** with the hardware device of **Ginter et al.** that included the run time limit being configured at least in part using license information associated with a protected intellectual property block implemented on a hardware device. The artisan would have been motivated because that would ensure the property providers proper compensation for the use of their electronic information; allow the potential customers to use the software in a demonstration mode (prototype operation) and use the full program features (production operation) for a limited time without paying license fee; and using a time based billing method, full use of the program for any period of time would be allowed.

DeRoo et al. does not expressly teach circuitry configured to disable the hardware device after the run time limit is reached by the clock. **Mueller et al.** teaches circuitry configured to disable the hardware device after the run time limit is reached by the clock (CL1, L50-52), because that allows a timer or score counting circuit to disable the hardware operation after a preset time limit or number of points scored (CL1, L50-52). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the hardware device of **DeRoo et al.** with the hardware device of **Mueller et al.** that included circuitry configured to disable the hardware device after the run time limit was reached by the clock. The artisan would have been motivated because that would allow a timer or score counting circuit to disable the hardware operation after a preset time limit or number of points scored.

27.2 As per claim 32, **DeRoo et al., Winkelman, Ginter et al.** and **Mueller et al.** teach the hardware device of claim 30. **DeRoo et al.** does not expressly teach that license information is associated with a time limit. **Ginter et al.** teaches that license information is associated with a time limit (CL2, L66 to CL3, L3; CL3, L18-22; CL47, L66 to CL48, L31; CL56, L25-29; CL59, L42-52; CL59, L62 to CL 60, L3; CL140, L25-34; use for a limited time), because that would ensure the property providers proper compensation for the use of their electronic information (CL2, L57-59); and allow the potential customers to use the software in a demonstration mode (prototype operation) and use the full program features (production operation) for a limited time without paying license fee; using a time based billing method, full use of the program for any period of time will be allowed (CL140,L25-38) . It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the hardware device of **DeRoo et al.** with the hardware device of **Ginter et al.** that included license information being associated with a time limit. The artisan would have been motivated because that would ensure the property providers proper compensation for the use of their electronic information; allow the potential customers to use the software in a demonstration mode (prototype operation) and use the full program features (production operation) for a limited time without paying license fee; and using a time based billing method, full use of the program for any period of time would be allowed.

28. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over **DeRoo et al.** (U.S. Patent 5,802,376), in view of **Winkelman** (U.S. Patent 4,435,752), and further in view of

Ginter et al. (U.S. Patent 5,892,900), **Mueller et al.** (U.S. Patent Re. 31,736), **Lin** (U.S. Patent 6,421,251), **Ngai et al.** (U.S. Patent 6,480,027) and **Watson et al.** (U.S. Patent 5,982,683).

28.1 As per claim 31, **DeRoo et al., Winkelman, Ginter et al.** and **Mueller et al.** teach the hardware device of claim 30. **DeRoo et al.** does not expressly teach that the hardware device is disabled using a reset of a register in the hardware. **Lin** teaches that the hardware device is disabled using a reset of a register in the hardware (CL55, L11-14; CL55, L55-57), because that ensures that the output signals are logic "0" thus removing the enable signal from the hardware register model (CL55, L11-14; CL55, L55-57). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the hardware device of **DeRoo et al.** with the hardware device of **Lin** that included the hardware device being disabled using a reset of a register in the hardware. The artisan would have been motivated because that would ensure that the output signals were logic "0" thus removing the enable signal from the hardware register model.

DeRoo et al. does not expressly teach that the hardware device is disabled using a global tri-state of the IO of the hardware. **Ngai et al.** teaches that the hardware device is disabled using a global tri-state of the IO of the hardware (CL7, L26-35), because that allows selectively driving signals from input pins or input/output pins or adjacent logic regions onto conductor segments or vice versa (CL7, L28-32). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the hardware device of **DeRoo et al.** with the hardware device of **Ngai et al.** that included the hardware device being disabled using a global tri-state of the IO of the hardware. The artisan would have been motivated because that would allow

selectively driving signals from input pins or input/output pins or adjacent logic regions onto conductor segments or vice versa.

DeRoo et al. does not expressly teach that the hardware device is disabled using a random failure within the hardware. **Watson et al.** teaches that the hardware device is disabled using a random failure within the hardware (CL6, L20-24), because the likely occurrence of a failure in random chance would be in the interconnect harness, the macrocells, the programmable logic and in the related products (CL6, L20-24). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the hardware device of **DeRoo et al.** with the hardware device of **Watson et al.** that included the hardware device being disabled using a random failure within the hardware. The artisan would have been motivated because the likely occurrence of a failure in random chance would be in the interconnect harness, the macrocells, the programmable logic and in the related products.

29. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over **DeRoo et al.** (U.S. Patent 5,802,376), in view of **Winkelman** (U.S. Patent 4,435,752), and further in view of **Ginter et al.** (U.S. Patent 5,892,900), **Mueller et al.** (U.S. Patent Re. 31,736), **Lin** (U.S. Patent 6,421,251).

29.1 As per claim 33, **DeRoo et al., Winkelman, Ginter et al.** and **Mueller et al.** teach hardware device of claim 32. **DeRoo et al.** does not expressly teach that the device is a programmable logic device. **Lin** teaches that the device is a programmable logic device (CL57, L28-35), because the programmable logic devices contain embedded array blocks and logic array

blocks which can be used to implement various memory and complex logic functions (CL57, L36-40). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the counter of **DeRoo et al.** with the counter of **Lin** that included the device being a programmable logic device. The artisan would have been motivated because the programmable logic devices would contain embedded array blocks and logic array blocks which could be used to implement various memory and complex logic functions.

Response to Arguments

30. Applicant's arguments filed on December 21, 2004 have been fully considered. In response to the Applicants' amendments to the independent claims 1, 22, 30, 34 and 54, the Examiner has used new references, **Schneck et al., Amano et al.** and **Ginter et al.**

Schneck et al. teaches a method for generating operationally limited software (Abstract, L7-17; Page 2, Para 0016; Page 4, Para 0044, Para 0045, and Para 0048; Page 10, Para 0154; Page 11, Para 0159); the method comprising:

identifying license information associated with a protected intellectual property block configured for implementation on a device (Abstract, L7-17; Page 2, Para 0016; Page 4, Para 0045, Para 0047 to Para 0050, Para 0052 to Para 0054; Fig. 3, Item 130; Page 6, Para 0097; Page 11, Para 0159);

generating operationally limited software, wherein the software is operationally limited using license information associated with the intellectual property block (Abstract, L7-17; Page

2, Para 0016; Page 4, Para 0045, Para 0048 to Para 0050, Para 0052, Para 0054; Fig. 3, Item 130; Page 6, Para 0097; Page 10, Para 0154; Page 11, Para 0159).

Amano et al. teaches a method for generating operationally limited hardware the method comprising: identifying license information associated with a protected intellectual property block configured for implementation on a device; generating operationally limited hardware, wherein the hardware is operationally limited using license information associated with the intellectual property block (CL7, L53-55; CL7, L65 to CL8, L8).

Ginter et al. teaches that the license information identifies a parameter associated with a prototype operation range and a production operation range (CL2, L66 to CL3, L3; CL3, L18-22; CL47, L66 to CL48, L31; CL56, L25-29; CL59, L42-52; CL59, L62 to CL 60, L3; CL140, L25-34; use for a limited time). **Ginter et al.** teaches that the run time limit is configured at least in part using license information associated with a protected intellectual property block implemented on a hardware device (CL2, L66 to CL3, L3; CL3, L18-22; CL47, L66 to CL48, L31; CL56, L25-29; CL59, L42-52; CL59, L62 to CL 60, L3; CL140, L25-34; use for a limited time).

Conclusion

ACTION IS FINAL

31. Applicants' amendments necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
April 1, 2005